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Development of Gate and Base Drive Using SiC Junction Field Effect Transistors

by Timothy E. Griffin

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14. ABSTRACT
A base drive and a gate drive were designed with 4*H*-SiC junction field effect transistors (JFET) and worked. Developmental JFET had uneven distribution of performance parameters. For example, the gate current (I_g) and voltage (V_{gs}) of each JFET required precise, customized control. This initial investigation designed and tested two JFETs into a base drive circuit board for an npn SiC bipolar junction transistor (BJT). The circuit rapidly drove a SiC BJT on and off with 4*H*-SiC semiconductor devices to perform to 150 °C. For the gate of an n-MOS or insulated gate bipolar transistor (IGBT) two other JFETs were designed into a drive circuit which worked. For these JFETs $I_d - V_{ds}$ curves and reliability degraded moderately with use.

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Contents

List of Figures

List of Tables

SiC Power Transistors: Focus on JFETs

Our JFET samples were received in April 2004 from Northrop Grumman, and most were rated for only moderate voltage and lower current. JFETs are basically less complex than other SiC transistors. Power transistors can block 600 V and are used as switches. In SiC different types are in early stages of development, compared to both Si ones and to reliable performance with controlled parameters. They switch at higher temperatures and have less *p*-*n* junction reverse leakage than Si devices. A typical Si power BJT cannot switch at 2 kHz, slower than a similar-current SiC BJT. A SiC power BJT conducts current across *p*-*n* junctions which can grow dislocations that reduce the conducting area and increase V_{be}; performance is less durable. V_{be} of SiC BJT is larger than for Si, but it would not be significant when handling high voltages and currents. A SiC gate turn-off thyristor has junction reliability problems, turn-off current gain less than three, much higher ratings, and hence few uses. Unlike the JFET, all MOS and IGBT are desirably and conveniently voltage-controlled. The thermal conductivity of low-doped *n*-type SiC (*1*) is 645.4 W $cm^{-1}(T - 132.8\ K)^{-1}$ and of high-doped 1669.1 W cm^{-1} $(T + 627.3\ K)^{-1}$, higher than for most other semiconductor materials.

New 1980 V and 50 A JFETs have dc I_d/I_g of many thousands, but with measured switching transient I_g their I_g is larger than for MOS. Unlike MOS, JFETs would also block some amount of negative V_{ds}; we do not find published V_{be} using this. Compared to other SiC power transistors, JFETs have worked to higher temperatures and frequencies, but lack very high conductance for power switches. SiC JFETs were sometimes called static induction transistors.

JFET Background

JFET and MOS have unipolar conduction without conductivity modulation by injected minority carriers as for BJT. Hence, compared to a similarly rated SiC BJT, a JFET has little switching power loss up to 10 to 50 MHz. This speed requires circuit designs that avoid excessive ringing. The JFET gate-to-source *p*-*n* junction depletion region at least partly pinches off its drain-to-source channel, which is of one conductivity type. A normally-on JFET needs V_{gs} to be negative to block all I_d, and positive V_{gs} to increase I_d; a normally-off JFET needs positive V_{gs} to conduct meaningful I_d. A JFET is compact and is not considerably degraded by problems with thermally grown SiO_2 (as is the MOS gate) and with the surface oxide passivation/ion implantation issues which reduce BJT base minority carrier lifetime and gain. JFETs are not heavily degraded like BJTs or other transistors by loss of emitter injection efficiency and doping and activation of different areas, or by surface recombination. Hence, JFET performance is potentially rugged; others operated with reduced mobility to 300 to 400 °C. Since the one *p*-*n* junction conducts

small or less I_g, JFETs should be more manufacturable than other transistors in SiC. Reliable future SiC BJT, MOS, or IGBT devices could exceed JFET conductivity, voltage, and probably current ratings. A JFET pinches off its channel; this controls I_d/V_{ds} conductance which decreases continually for increasing V_{ds}, unlike a Si MOS or BJT which has much less drift resistance than source resistance. When V_{ds} equals the pinch-off voltage, the depletion layers almost meet at the drain and the conduction electrons move at the maximum drift velocity, so I_d saturates. V_{ds} preferably exceeds V_{gs} at low I_d so that the drain does not receive current from the gate.

Our JFET I_d–V_{ds} exhibited less shift or degradation than previous BJT do. After initial turn-on JFET gate-source junction charging, our I_g are undesirably continuous at a few μA to a few mA but are still smaller than the BJT I_b. Our JFET V_{gs} must be controlled within a narrow range. This is less convenient or desirable than for other transistors. Present JFET manufacturing may lack yield with adequately narrow variation of the I_g–V_{gs} and the I_d–V_{ds} curves. V_{gs} of normally-on JFET #407 was tested to –35 V but some SiC JFET (*2*) withstand only –23 V, still larger than the specified –12 V breakdown for Si normally-off JFET Qspeed LD1010DA.

A cascode consists of a bottom low-voltage-rated normally-off JFET and a top high-voltage-rated normally-on JFET. Control and switching performance are improved over a single JFET. Control is applied to the bottom JFET's gate, and the bottom drain is connected to the top source. The top gate is connected to the bottom source and to ground. The top drain is connected through its load to its power supply. A cascode is normally-off for safety and easier control. For its higher I_d rating it withstands notably higher V_{ds} than one JFET, like a MOS, but we did not need these ratings. When V_{gs} is fully-on, we measured a cascode to have I_d increasing much faster with the initial increase of V_{ds} than a JFET and saturating within a smaller range of V_{ds}. New normally-on power JFET are now usually in a cascode. Our cascode samples were unsuitably packaged for 150 °C and so were not used.

A normally-off JFET has a narrow or a low-doped channel which reduces on-state conduction and current density; it operates in enhancement-mode. Others report its lower change in V_{gs} than a MOS may compromise its immunity to a couple of volts of noise (*3*). Most JFETs, including ours, are vertical for higher current density, denser packing, and lower on-resistance than a lateral, which could be monolithically integrated. The drift region's bulk electron mobility varies as $T^{-1.5}$ so JFETs share current well in parallel. To 150 °C our V_{gs} decreased less than 10%. Some JFETs operate with junction to 300 °C; to 375 °C (*4*) one normally-on JFET was designed so its I_d decreased only 20% and its threshold V_{gs} decreased 0.4 V above 250 °C.

An (*5*) optocoupler driving a JFET half-bridge at 150 kHz PWM (*6*) self-adjusted for normally-on JFET $I_g(V_{gs})$ variations and saw reduced dV_{gs}/dt = 50 kV/μs for JFET at 25 °C. Negative drive put the JFET gate junction at the beginning of reverse-biased avalanche; we question durability.

JFETs (*4,7,8*) should be rugged. If a JFET overheats, the current saturation with temperature gives brief protection (*9*). The future should have improved *p*-*n* junctions, better SiC material,

superior device design, and fabrication for durability. Optimistically gate-source capacitance would be less than ours.

JFETs Used, and Circuit Using Normally-Off JFET to Drive BJT On

Our JFET parameters were uneven, but few had excessive I_g. For at least one temperature and V_{gs} a few had a hump to an unacceptably low I_d then decreased. The 371B curve tracer measured using I_g above a few mA from power supply Agilent E3648A to monitor accurately V_{gs}. The dc I_d divided by the controlling V_{gs}'s dc I_g rapidly declined with V_{gs} from initially more than 3/0.001 to our minimum 5/0.1, but was always larger than BJT gain values.

Each JFET was switched as fully as feasible to 150 °C. The drive circuit to 150 °C controlled forward V_{gs} so that it was large enough for adequate V_{ds}/I_d conductivity but small enough so that dc I_g was not large and rising sharply. The dc I_g was usually much smaller than our upper limit of 100 mA; new devices would use less. A brief and somewhat larger I_g provides modest charge-up of the gate-source junction. The reverse V_{gs} must be sufficiently negative to keep a JFET off with sufficiently small leakage. Each of our drive designs had two JFETs chosen for measured $I_d - I_g - V_{gs}$ characteristics.

Current ratings of the JFETs were 5 A to 20 A, less than for SiC BJTs. Our highest JFET V_{ds} rating was 500 V for normally-off 54 and needed its gate driven sufficiently negative to minimize leakage. Some of our normally-off JFETs, even at their largest listed negative V_{gs}, had V_{ds} rated merely a few tens of volts. JFET I_d increased with positive V_{gs} until almost I_g = 100 mA, and decreased to negligible at more negative V_{gs} and low I_g. At fully-on V_{gs} the JFET I_d conducts after V_{ds} = 0 V except JFET #80 at 0.8 V, but one cascode began at 0.4 V. Importantly, this cascode had a smaller incremental series resistance 0.17 Ω to 8 A, while cascode 80 was 0.2 Ω near 4 A at 1.6 V, reaching 8 A at 4 V. A 3 mm by 6 mm fully-on BJT #C2 levels out at 15 A at 0.9 V. JFET I_d was gradually leveling out at V_{ds} = 4 V and reached its maximum near 6 V. Unless highly derated, a JFET has conduction power loss several times higher than for a BJT.

The drive for the BJT used normally-off 414 and normally-on 505. The drive for the MOS switch used normally-off 407 and 411. Table 1 lists measured I_d and I_g values before use.

Table 1. JFETs 407 and 411.

V_{gs} (V)	I_g (mA)	V_{ds} (V)	I_d (A)
JFET 407: 1.4		5	on <0.00005
1.6		5	0.0016
2.2		5	on
2.5	2		
2.6	20		
2.65	50		
–10	0		

Table 1. JFETs 407 and 411 (continued).

2.5	140	0.02	
2	110	1	
1.8	5	1	
1.6	0.09	1	
JFET 411: 0		30	<0.000001
2		0.5	0.25
<2.5	a few		

Our base drive supplied a positive V_{be} for turn-on and a smaller negative V_{be} to speed turn-off and to increase the margin against turn-on during inverter transients or noise. This margin is also needed during BJT turn-off when constriction of the current gives large horizontal current density as the emitter contributes to V_{be} (*10*).

Specific JFETs were selected for their $I_d - V_{ds} - V_{ds}$ curves, then the drive circuit was designed for these JFETs. Among our older, not highly durable developmental SiC BJT like in our tables 3, 5, 6, and 8 V_{be} varies notably, so a particular BJT must be chosen. The drive for the BJT base was first on, with a duty cycle averaging near 50%. Its source through series resistors supplied the BJT's I_b at its V_{be}. Subsequently at less I_d a normally-on JFET 505 connected at its drain was used to reverse-bias the base-emitter junction and remove more rapidly the p_{base} carriers for turn-off. This shortened the duration of turn-off I_c thus reducing the switching energy loss. V_{be} swung between a maximum of 3.5 to 4 V and a minimum of –1 to –1.6 V, which is tolerable for the SiC BJT used in this design. The drive could control one BJT as in an inverter producing 480 V_{rms}.

The JFETs were mounted on electrically insulating and thermally conductive AlN ceramic and Electrolube HTSP heat sink compound. This was placed on a heater block 5.73 cm square above the circuit board with a WS-81 RTD thermistor in one corner. An optocoupler with resistors drove each JFET V_{gs}. The two optocouplers were Avago HCPL-3180 receiving power between V_{cc} and V_{ee}. The normally-off JFET's optocoupler's output drove the JFET's gate with I_g usually negligible at V_{gs} nearly 2.3 V. A Tektronix AFG310 or Agilent 33220A function generator gave a pulse of 2.4 V and 13 mA to the optocoupler input for 1.55 V at 13 mA, then –3 V. Optocoupler of normally-off JFET had output 7.9 V into at least 50 Ω to ground.

Initially the pulse generator gave positive signal to drive the BJT on, 0 V for the circuit's observed 1 µs settling, negative for at least 1 µs, then 0 V for another 1 µs. The drive should follow 25 µs pulses. Different optocouplers and JFETs did not share power supplies, reducing cross-talk interference. Selectable resistance from the JFET source to the BJT base controlled I_b. Our turn-off negative voltage drive was not through the base resistor and hence did not bypass it with a Schottky diode. Measurement of JFET 414 is in table 2.

Table 2. JFET 414.

V_{gs} (V)	V_{ds} (V)	I_d (A)
25 °C: 2.2		0.9
2.3 to 2.35	1	3
	2	4
	3.9	5
50 °C: 2.3 to 2.35	3	5
150 °C: on	1	3.5
on	2	5
2.3 I_g = 35 mA, <2.4 135 mA		

After subtracting 1 V V_{ds} and 2.9 V V_{be}, we calculate 6.1 V through the output base resistors. Series resistor 10 Ω gives I_b = 0.6 A, 5 Ω gives 1.2 A, and 2.5 Ω gives 2.25 A at V_{be} = 3.37 V. For 10 V – 1 V V_{ds} – 3.52 V V_{be} (for 3.26 A) = 5.48 V through 1.67 Ω calculates 3.26 A; for 1 Ω 10 V – 1.12 V – 3.88 V (for 4.7 A) = 5 V is 5 A. SiC BJT module (#9-28) measured at V_{be} = 2.8 V to begin significant I_b and at 2.95 V I_b = 1.4 A. I_b = 0.5 A gave I_c = 13 A. SiC BJT chip #C706 of July 2006, was 0.5 cm square, so Cree's probe card pulsed at 50 A but we pulsed to 20 to 25 A. Its measured $I_b(V_{be})$ at 25 °C is in table 3.

Table 3. SiC BJT chip #C706 $I_b(V_{be})$.

V_{be} (V)	I_b (A)
2.91	0.5
3.073	1
3.31	2
3.52	3
3.73	4
3.88	4.675

Figure 1 is the base drive circuit without some stiffening capacitors and the normally-off JFET's later C_{gs} = 1.2 nF and finally-added C_{ds} = 2 nF.

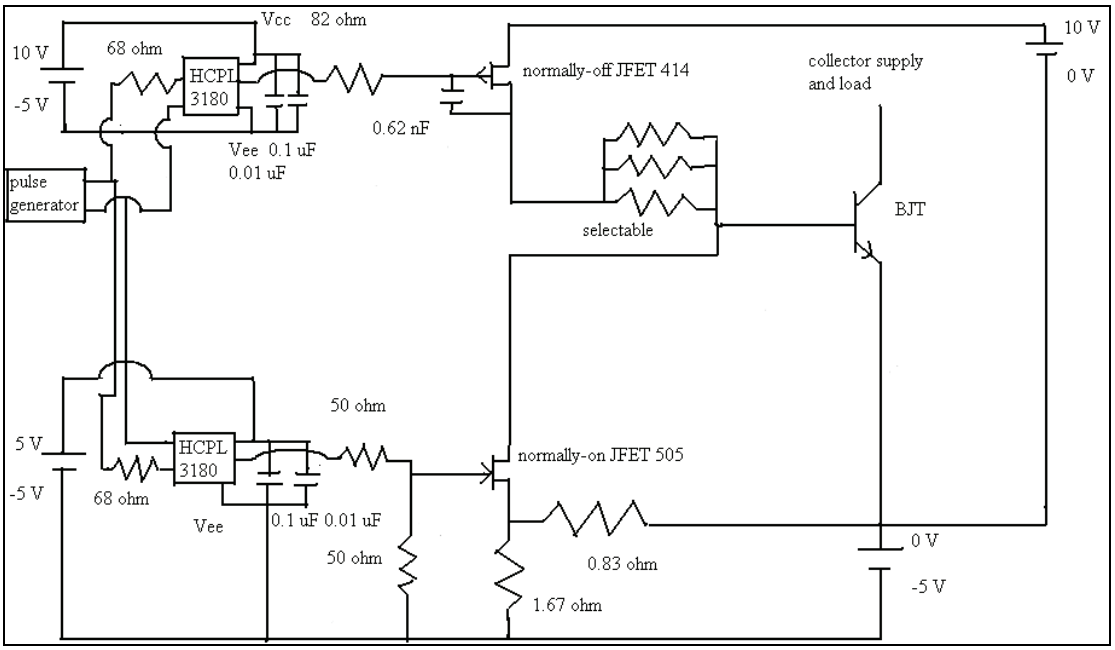

Figure 1. JFET Drive Circuit for BJT base.

Capacitors in parallel stiffen each power supply voltage. An optocoupler's supply had two 0.1 µF and needed a 4.7 µF. A JFET's power supply needed an 82 µF and a 4.7 µF for 1 A, and also had 150 µF and two 0.1 µF. With the normally-off JFET V_{gs} near 2.35 V (limited by I_g at 150 °C), we needed all of V_d = 10 V for adequate V_{gs} so I_c would rise fully for adequate I_b and V_c, and so V_{dg} was more than 0 V. To reduce ringing during the fall of V_{gs}, we added to the normally-off JFET an external C_{gs} = 0.62 nF, not a lone C_{ds} which would cause V_{gs} to swing too far.

Part of Base Circuit for Normally-On JFET to Drive BJT Off

This part of the driver supplies a negative V_{be}. The normally-on JFET 505 is driven by a signal to the optocoupler input cathode (the reverse of usual) with signal generator ground connected to the optocoupler input anode, so a negative signal turns on this JFET's optocoupler. First our normally-off JFET supplies I_b, followed by at least 1 µs deadtime, then conduction by the normally-on JFET reverse biases V_{be}. When the normally-on JFET was on, the normally-off JFET 414 at V_{gs} = 0 V had no leakage at V_{ds} up to 6 V. Measurement of JFET 505 is in table 4; at V_{gs} less than –1.1 V the JFET withstood V_{ds} = 3 V, allowing the normally-off JFET to supply I_b.

Table 4. Normally-on JFET 505.

V_{gs} (V)	I_g (mA)	V_{ds} (V)	I_d (A)
25 °C: 2.38	0.4		
2.735	100		
to -5	none		
0		–3	0.036
–0.8		–3	0.00315
–1		–3	0.0005
150 °C: –3	0.001	10	0.000009
–2		10	0.00005
0		3	0.04
0		4	0.65
1.8 on			
1		1	1/3, out of BJT base

The normally-off JFET when conducting made V_{be} at most 3.3 V; this potential plus 1.67 V gave 5 V JFET drain, hence V_{ds} = 5 V and V_{gs} = –1.9 V produced negligible leakage.

In the BJT base drive, V_{ds} of the JFET began to rise at 0 s, then at 0.5 µs I_g reached 780 mA and at 4 µs 920 mA large for charging the C_{gs} of the gate-source *p-n* junction toward forward conduction, notably a peak not far smaller than I_d and more charge than for a MOS. I_d rose linearly over 2 µs to 3 A, then at 3.4 µs reached 4.6 A. When V_{ds} rang slightly through 0 V, I_g immediately became much smaller. After 1.2 to 2.1 µs later the turn-off normally-on JFET V_{gs} turned on, then V_{be} was less than –2 V and all voltages and currents were acceptably off-state with reduced ringing.

For a collector supply of 20 V through a 1 Ω load, I_c settled in 14 µs. The BJT base drive switched acceptably. The two 9 A SiC BJTs mounted on a 2.54 cm AlN square switched with a gain of 20.

Base-Emitter Voltage and BJT Examined to High Temperature

A SiC 1200 V, 50 A BJT received in early 2006 from Steven Kaplan and Aderinto Ogunniyi is shown in table 5. Its V_{be}, changing little with temperature, is notably almost two times as large and not the expected smaller compared to that of table 6's smaller BJT at 25 °C for the same I_b.

Table 5. SiC BJT 50 A $I_b(V_{be}, T)$.

I_b (A)	V_{be} 25 °C (V)	V_{be} 100 °C (V)	V_{be} 150 °C (V)
0	4.8	4.7	4.5
0.5	5.6	5.6	5.5
1	6.0	5.9	5.8
2	6.3	6.3	6.2

Table 6. SiC BJT 10 A $V_{be}(I_b, T)$.

I_b (A)	V_{be} (V): 25 °C	V_{be} 100 °C	V_{be} 150 °C	V_{be} 200 °C	V_{be} 250 °C	V_{be} 300 °C
0	2.7	2.55	2.48	2.32	2.25	2.20
0.5	3.22	2.94	2.77	2.69	2.54	2.44
1	3.45	3.10	2.92	2.81	2.68	2.56
2	3.75	3.41	3.17	3.02	2.89	2.75

Table 6 shows the $V_{be}(I_b, T)$ of a 10 A SiC BJT (*11*). We calculate the output requirements for the normally-off JFET 414 based on these data. At 25 °C for I_b = 0.5 A at V_{be} = 3.22 V and (at V_{gs} = 2.2 V) V_{ds} = 0.2 to 0.3 V leaves 6.5 V across the resistors, so they would be 13 Ω and absorb most change in V_{be}. At 150 °C V_{be} = 2.77 V leaves around 7 V for I_b = 0.54 A. For I_b = 2 A at 25 °C V_{be} is 3.75 V, and (at V_{gs} = 2.2 V) V_{ds} is around 0.8 V; these left 5.45 V across the resistors so they would be 2.73 Ω. At 150 °C V_{ds} = 1 V left about 5.83 V across the resistors for I_b = 2.13 A. The smaller resistor for I_b = 5 A would give poorer regulation.

Table 7 shows the drive's JFETs at higher temperature speeded up some and drove V_{be} to 3.25 V.

Table 7. Base drive's speed with JFETs at temperature.

V_{ds}	JFETs at 25 °C	JFETs at 100 °C	JFETs at 150 °C
11.5 V to 3.5 V initial fall	334 ns	256 ns	230 ns
Rise	620 ns	200 ns	192 ns
settles to 12 V in	1500 ns	640 ns	500 ns
I_b at 18 µs	0.87 A		0.82 A

Additional SiC BJTs were a bottom BJT and a top BJT 0.3 cm square chip with dark brown encapsulant (Cotronics 4460 with 15% 102 Resbond flexibilizer) mounted together on a 2.54 cm square AlN and measured in table 8. Cree pulsed each to 20 A; we did not exceed this and usually were within 10 A dc. The bottom BJT's V_{ds} initial fell in 328 ns and rose in 264 ns then had ringing, but reached 12 V faster than Si could; I_b at 18 µs reached 0.935 A.

Table 8. SiC bottom and top 20 A BJT $V_{be}(I_b)$.

I_b (A)	V_{be} bottom BJT (V)	V_{be} top BJT (V)
0.1	2.63	2.75
0.5	2.99	2.955
1	3.23	3.16

With collector load of 1 Ω when the BJT turned off with I_c = 7 A, 0.4 A of ringing was observed. We reduced the turn-off speed with external mica C_{gs} and C_{ds} to reduce ringing and to increase transient margin for V_{be}. The normally-off JFET needed at least its original C_{gs} = 0.62 nF to reduce ringing during falling edge of V_{gs}. During the negative V_{be} pulse reached a minimum of –0.82 V for adequate noise margin. The normally-off JFET V_{ds} had minor ringing. The 0-90%

turn-on switching power $V_{ce}I_c$ was 2.7 µJ during 350 ns. At turn-off the switching energy was 2 µJ during 124 ns.

We chose C_{gs} = 1.2 nF and C_{ds} = 2 nF. Subsequent measurements found turn-on V_{be} overshoot was 0.72 V, and that there was little overshoot for V_{gs} or I_b. At turn-off, V_{ce} rang by 3.6 V. V_{be} also acceptably decreased at 250 ns to less than 1 V, at 460 ns to 0.4 V, and at 1000 ns to near 0 V.

Further Testing of JFET Drive for BJT

Switching data for JFETs alone being at higher temperature in table 9 show this gave V_{be} more noise margin.

Table 9. Switching with base SiC JFETs alone at temperature.

	JFETs 22 °C	**100 °C**	**150 °C**
I_b (A) at turn-on	0.36	0.37	0.384
I_b (A) 80 ns later	0.27	0.29	0.29
I_b (A) 300 ns later leveled	0.35	0.37	0.38
I_b (A) ending at	0.37	0.395	0.4
V_{be} (V) at turn-off during the negative pulse	–0.95	–1.2	–1.43

For an inductive load to simulate a motor we tried 33 µH in series with 1 Ω. This gave much less current and sometimes severe high-frequency oscillation, in only a few minutes surprisingly causing damage to the bottom BJT.

Table 10 is for the top SiC BJT switched with a resistive load at 40% duty cycle. Notably I_c turned on much faster than for a Si BJT, and turned off even faster. For this couple of seconds of continuous run, heating decreased I_c slightly. At turn-off for the sixth row I_c was immediately 1.44 A then in 3 µs was 0 A; the last row was immediately 1.26 A then in 2.5 µs was 0 A.

Table 10. I_c and I_b for top SiC BJT.

Through load	**Power supply (V)**	**I_c peak (A) after rising for (ns)**	**I_c (A) 2 µs after peak, as for PWM**	**I_b (A) at 550 ns rise time**
1 Ω:	8	7	6.2 at V_{ce} = 0.4 V	base **11 Ω**: 0.61
0.4 Ω:	4	8.4	7	0.59
	5	10	8.8	0.58
	6	12	10.8	0.575
	7	12.6	12.4	0.57
	8	11.8 (at 450 ns)	12.3, average current gain 21.6	0.57 (0.4 at 72 ns, 0.5 at 200 ns)

Table 10. I_c and I_b for top SiC BJT (continued).

	8	15.6 (at 1170 ns, 12.8 at 450 ns)	14 at V_{ce} = 1 V	base **6 Ω**: 0.97 (0.24 at 72 ns, 0.77 at 200 ns, 0.92 at 550 ns), fan on BJT
	change range 10	18.2	16.5	0.89 (0.144 at 72 ns, 0.673 at 200 ns, 0.82 at 550 ns)
	11	20.1	18.6 (V_{be} = 4.2 V)	0.9 (0.192 at 72 ns, 0.65 at 200 ns, 0.84 at 550 ns)
1 Ω:	15	13.0 (at 1480 ns, 12.0 at 450 ns)	12.7	0.92 (0.19 at 72 ns, 0.66 at 200 ns, 0.89 at 550 ns)
	20	17.2 (at 1240 ns, 16.1 at 450 ns)	16.6 saturating with I_b	0.9 (0.2 at 72 ns, 0.593 200 ns, 0.84 at 550 ns)

Figure 2 has channel 1 I_c, channel 2 I_b, channel 3 V_{be}, and channel 4 V_{ce}. After I_c had mostly turned off, it rebounded, from 0 to 1 µs totaling charge of 1.1 µC. From 1 to 2 µs total charge was 1 µC, and from 2 to 3 µs 0.4 µC. A shorter dead-time might not work between turn-off of the normally-off JFET and turn-on of the normally-on JFET for negative V_{be}. Our higher pulsed I_c damaged the top developmental SiC BJT.

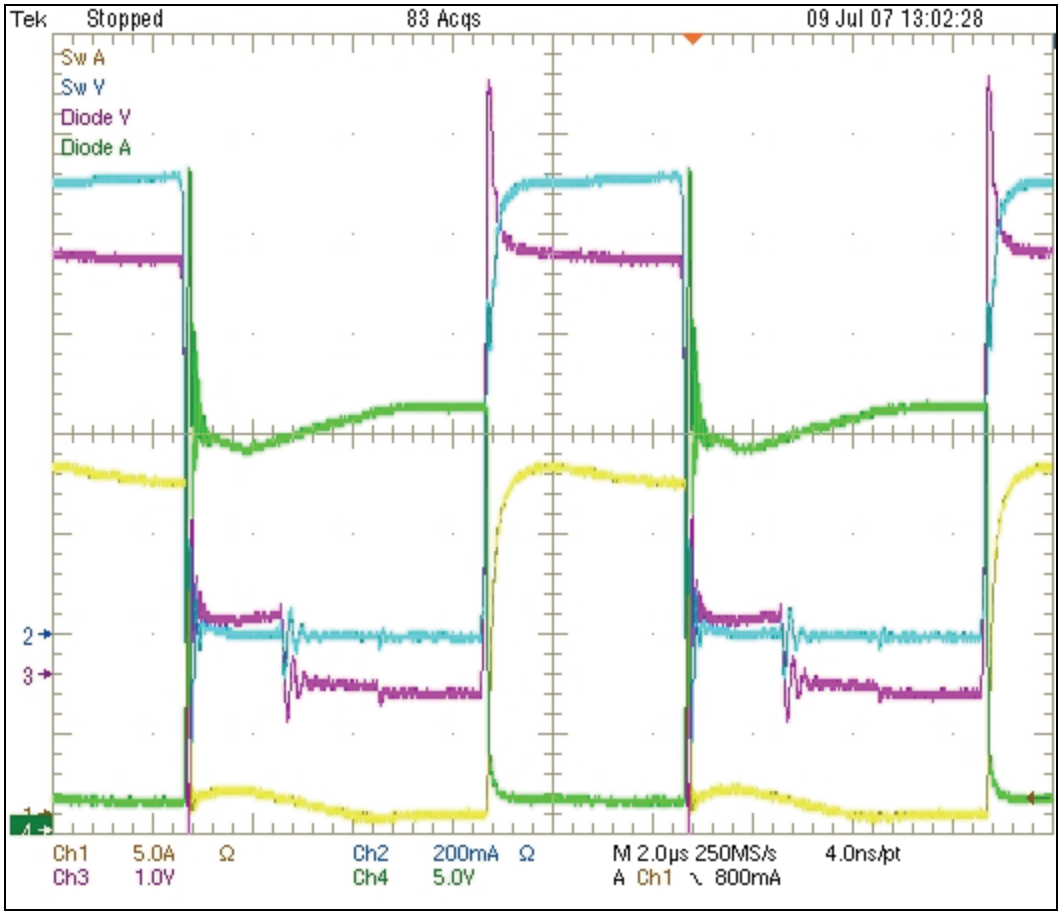

Figure 2. Oscilloscope Trace of Switching of Top SiC BJT.

We changed to a Si 2N5885 BJT with two MUR4100E in series to its base simulating SiC V_{be}. To conduct negatively at turn-off, we added a 10 A leg of a Cree Schottky diode C2D20120 anti-parallel to the two MUR4100E. After a 16 µs positive drive, I_c leveled out. From 2.04 µs to 14.1 µs our negative I_b = –5.1 mA removed a notable 62 nC reducing V_{be} to 0.42 V, then V_{be} decreased more rapidly. Presumably capacitance caused V_{be} at the beginning of negative drive to jump upward by 0.3 V, and at the end of negative drive to suddenly jump downward by the same 0.3 V to a final potential of –1.1 V.

Moderate current degradation of the two JFETS by this operation mostly at room temperature is shown in table 11.

Table 11. JFET degradation.

V_{ds} (V)	V_{gs}(V)	I_d (A) initial July 2006	I_d (A) present
JFET 505: 7	0	0.08	0.036
7	–0.2	0.07	0.004
3.7	1	2.42	1.9
JFET 414: 0.6	2.3	1.93	1.3
1.3	2.3		1.9
2.1	2.1	1.09	0.82

This degradation did not notably affect our on or off operating points, but is still undesirable. This presumably caused the JFETs to sometimes initially provide insufficient I_b. Production devices would need a smaller *I-V* change to high temperature with use. $V_{supply\text{-}emitter}$ was an adequately stiff 36 V through 2 Ω, but presumably this degradation caused the rise in I_c to become more gradual. Heating over a couple seconds changed its initial shape.

$V_{source\text{-}emitter}$ of the normally-off JFET already had external C_{gs} = 1.2 nF in order to counteract degradation; for this we now added C_{ds} = 2 nF. For table 12's second row the normally-off JFET $V_{source\text{-}e}$ during dead-time was 1.6 V; the diodes and base-emitter junction had forward charge. Then during negative drive it was –0.2 V until V_{be} went negative, then it followed V_{be}. The last row shows that the negative drive needed to be at least 20 µs, and at its beginning the degradation of JFETs had begun to obscure the V_{be}'s jump upward of a few tenths of a volt. When the negative drive ended, the normally-off JFET's C_{gd} must have caused $V_{source\text{-}e}$ to jump from –1.7 V to –1.98 V. I_b while averaging –2 mA removed 21 nC. The I_c of 2N5885 repeatedly rose in 10 µs to a stable 20 A, and fell at 13 µs to 2 A (V_{ce} reached 96 % of supply) and at 16 µs to 0 A. JFET degradation stopped the testing.

Table 12. Later Si BJT switching.

Positive drive time (µs) then 2 µs dead-time	Negative drive time (µs)	I_c and its turn-off swing (A)	Initial V_{be} (V)	V_{be} after neg drive (V)
16	24	16.5 –1.5	–1	jump to –1.3
20	30	18.3 –1.6	–1	jump to –1.3
25	15 too-brief	19.2 –1.7	–0.18	not change
30	10 too-brief	21 –1.1	0.5	in 200 µs 0.3 V
single shot 30	20 adequate	18 –0.9		still from –1.1 jumped to –1.38

Circuit to Drive MOS Gate

We designed a drive for a SiC nMOS or IGBT in an inverter. We drove a Si MOS DE475-102N21A from IXYS Corp., rated to 30 MHz and 24 A with gate charge 160 nC (gate-to-source 35 nC). The MOS gate drive circuit is in figure 3 without some stiffening capacitors.

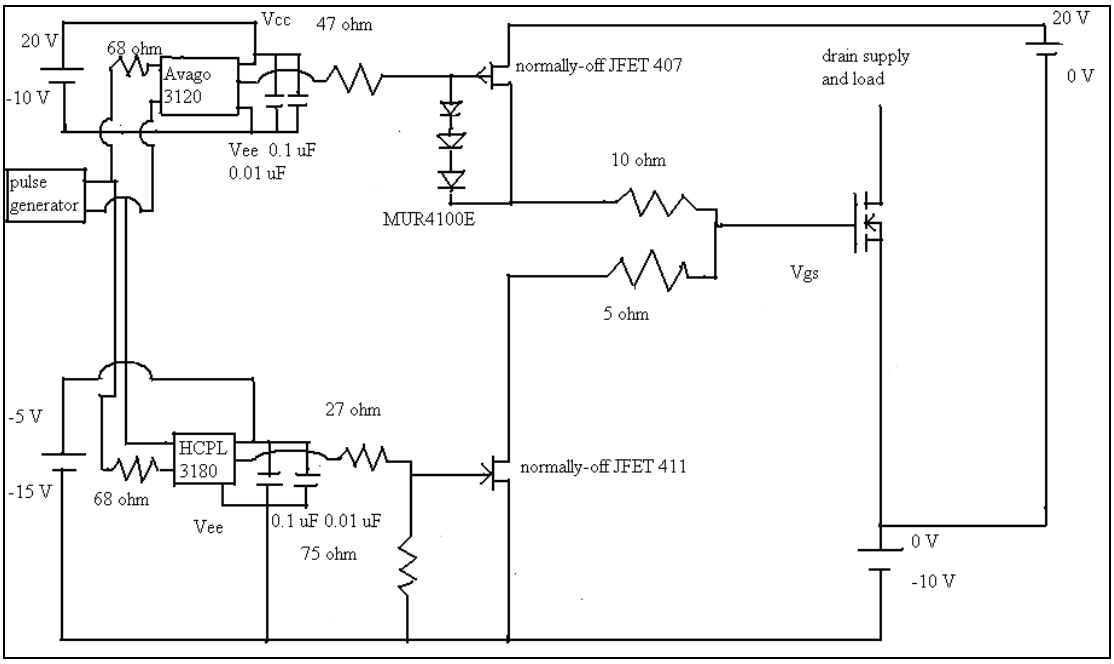

Figure 3. JFET Drive Circuit for MOS Gate.

The drive for a MOS gate requires a much larger MOS V_{gs} swing from 20 V to –10 V than for a BJT base, but requires only a brief I_g to charge or discharge the MOS Q_{gs}. The change in JFET V_s was similar to the change in MOS V_g. The turn-on JFET 407 drove the MOS V_{gs} to nearly 20 V. From gate to source three MUR4100E diodes in series (equivalently one leg of a Cree CSD20120D) conducted at excessive JFET V_{gs} to reduce V_{gs}. The turn-on JFET's V_{gs} swung to –30 V, similar to SiC JFET articles.

The turn-off JFET was normally-off 411 and drove the MOS V_{gs} to –10 V. The drive signal was such that both JFETs were off for a dead-time of at least 0.4 µs but typically above 2 µs. Next the turn-off JFET was on, then both were off for 2 µs, then the turn-on JFET was on. The MOS I_g for turn-on from –10 V to 20 V approximated a 1.6 A triangle 300 ns long and for turn-off a –1.1 A triangle 500 ns long, or approximately 250 nC.

In a breadboard circuit the turn-on JFET switched the MOS on, then during the dead-time the MOS V_{gs} fell by an insignificant 1 V until the turn-off JFET turned it off. The MOS V_{gs} was switched rapidly. The part of turn-on from –10 V to 0 V (with MOS I_g = 1.46 A, 1.6 A peak at

16 ns later) totaled 56 nC in 87 ns. From 0 V to 15 V with 1 A, the charge was 189 nC in 134 ns, and from 15 V to 20 V there was 58 nC in 121 ns. The JFETs switched rapidly. The MOS received positive then negative I_g; the MOS V_{gs} stabilized with minor ringing. The part of MOS turn-off from V_{gs} = 19 V to 14 V with I_g = –0.7 A was –23 nC in 85 ns, from 14 V to 0 V with –1.0 A was –147 nC in 152 ns, and from 0 V to –10 V was –110 nC in 201 ns.

The turn-off JFET's I_g, with peak 108 mA, totaled 10.6 nC in 554 ns, initially for JFET gate-source capacitance during the beginning of the negative drive. During the end of negative drive JFET I_g with peak –120 mA totaled –6.1 nC in 125 ns, almost all for JFET gate-source capacitance.

Conclusions

Developmental SiC JFETs were used since they controlled their I_d current using an I_g smaller than a comparable BJT's I_b, had plenty of speed, were short-term durable, and were available. Fabrication of these JFETs had not controlled their $I_d - V_{ds} - V_{gs}$ curves and parameters to within narrow limits. Two JFETs in a cascode can notably improve ratings and control. JFETs work now to higher temperatures than other power transistors. The custom narrow control of these JFETs is more difficult; they are not current-controlled like BJT and do not stay conveniently voltage-controlled like MOS. MOS and BJT will have lower resistance and voltage drop and more familiar performance.

Designing with desirable design parameters, we chose a specific normally-off JFET to drive a SiC BJT base on and a specific normally-on JFET to drive it off. For the initial investigation, a circuit board was designed and tested. These JFETs operated rapidly and effectively at temperatures up to 150 °C. The circuit was adjusted for less ringing. The $I_d - V_{ds}$ curve (for constant V_{gs}) degraded moderately with use. Similarly two normally-off JFETs were chosen to drive a MOS gate, and the circuit was designed and performed well.

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